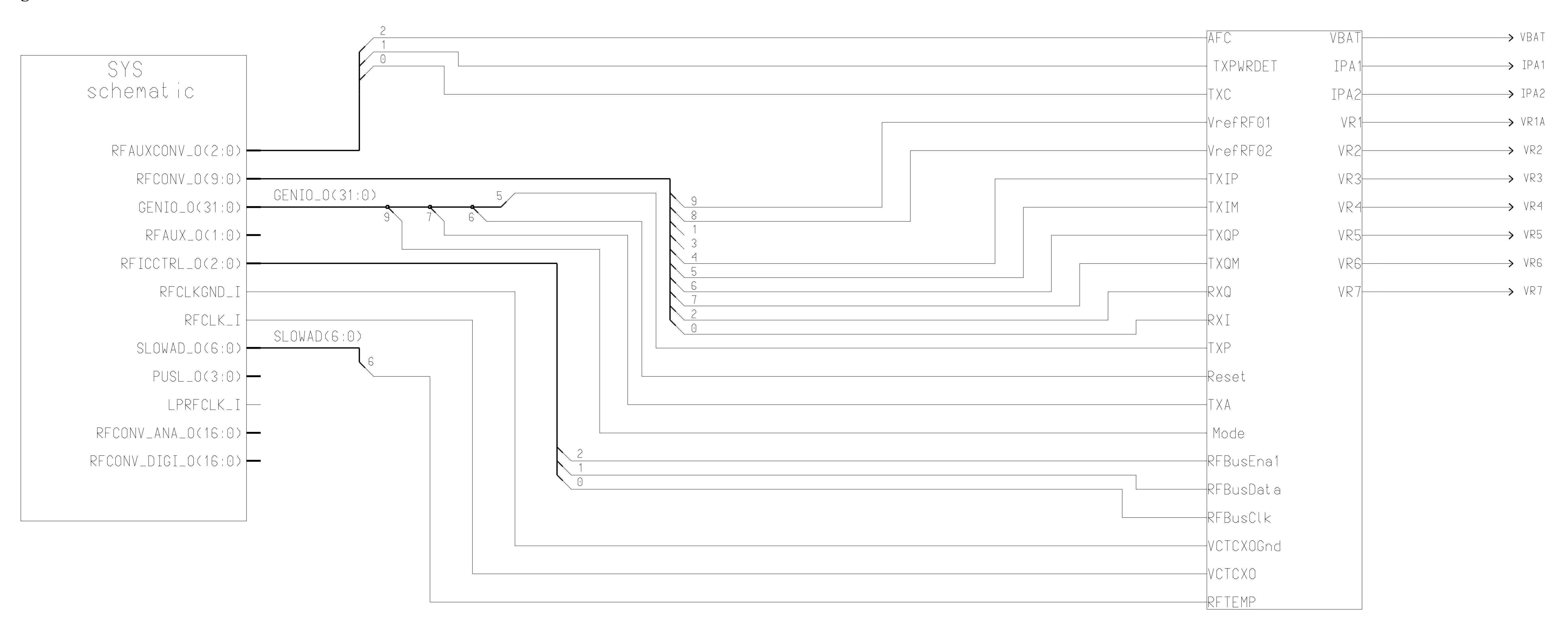
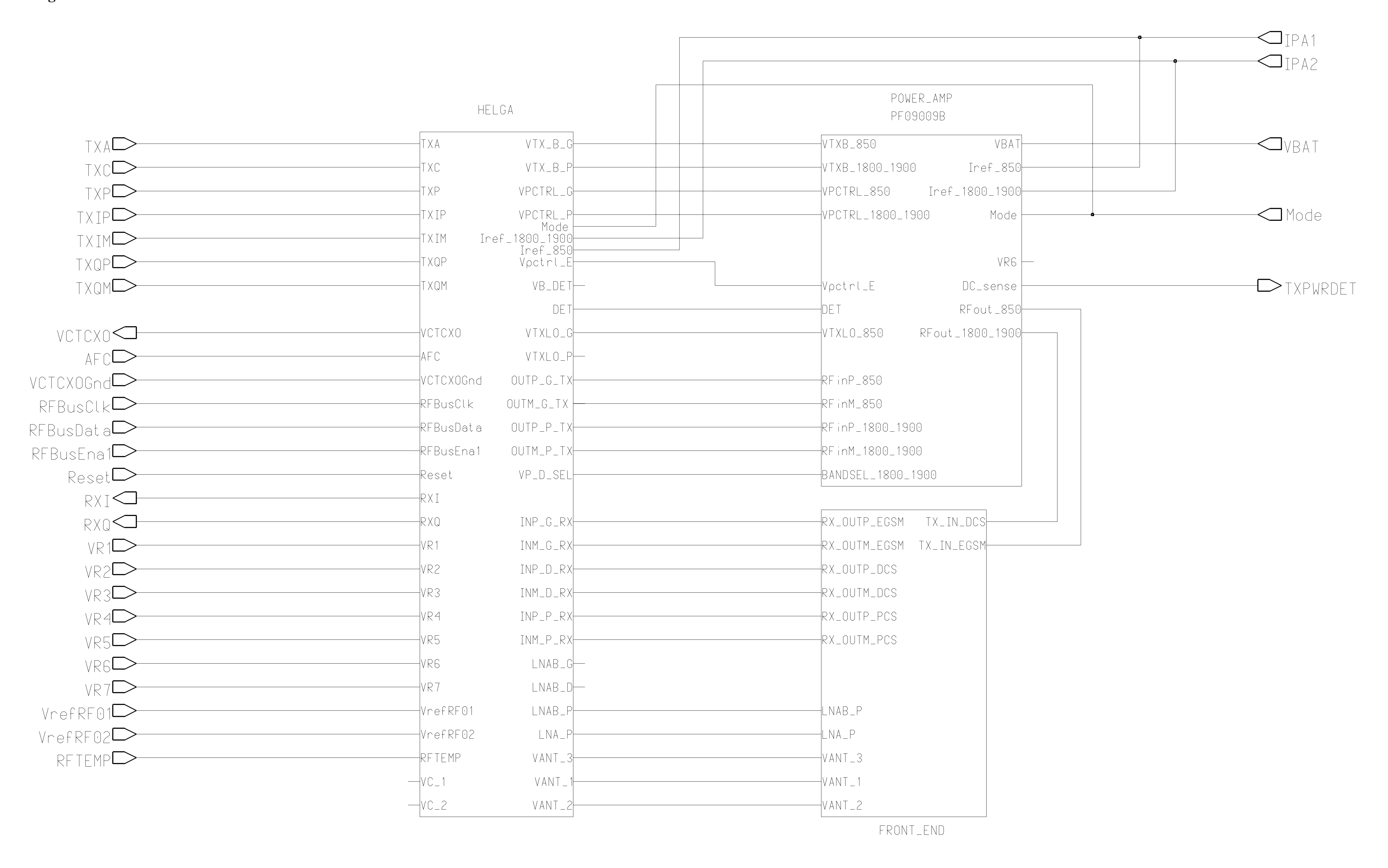
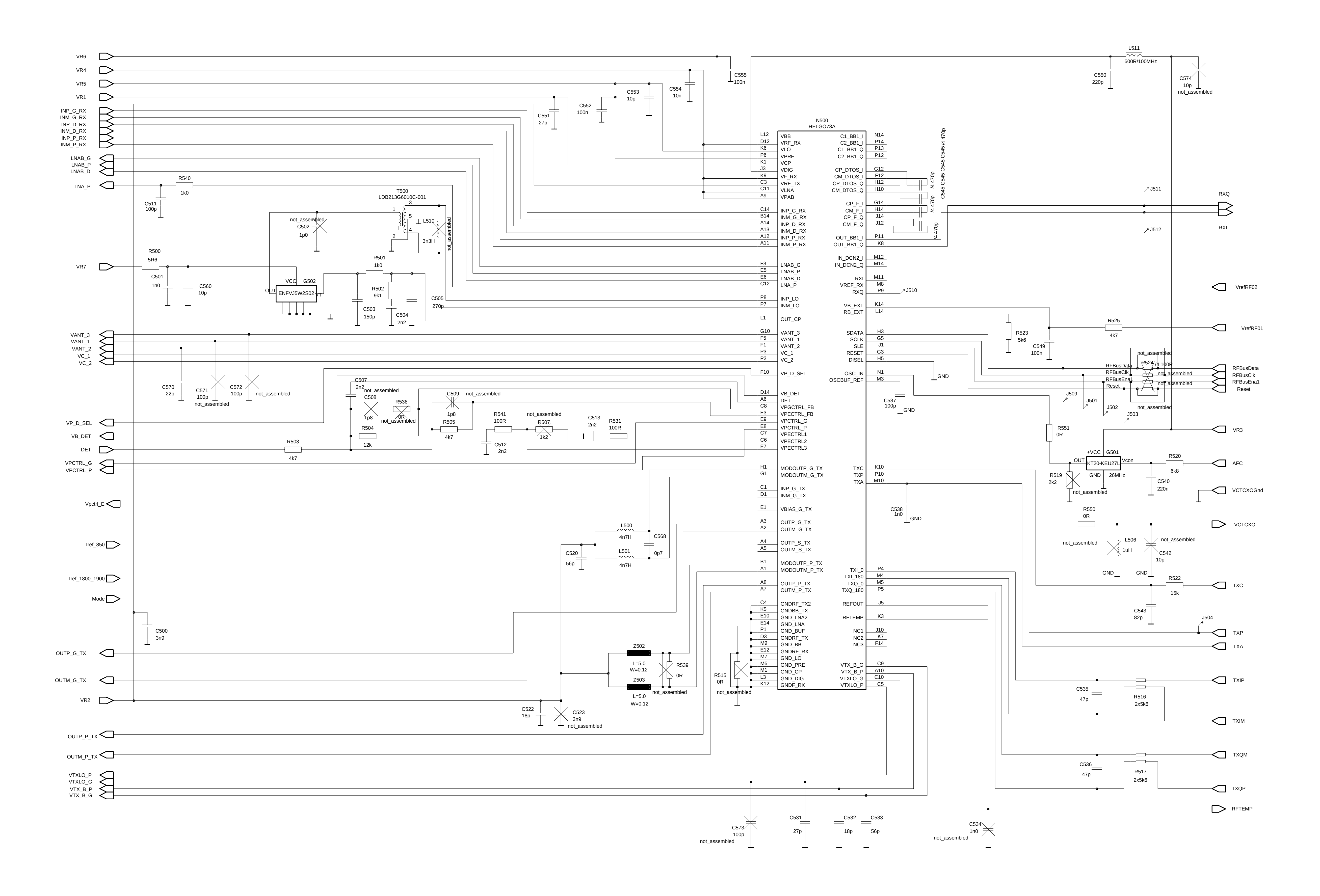
Block diagram



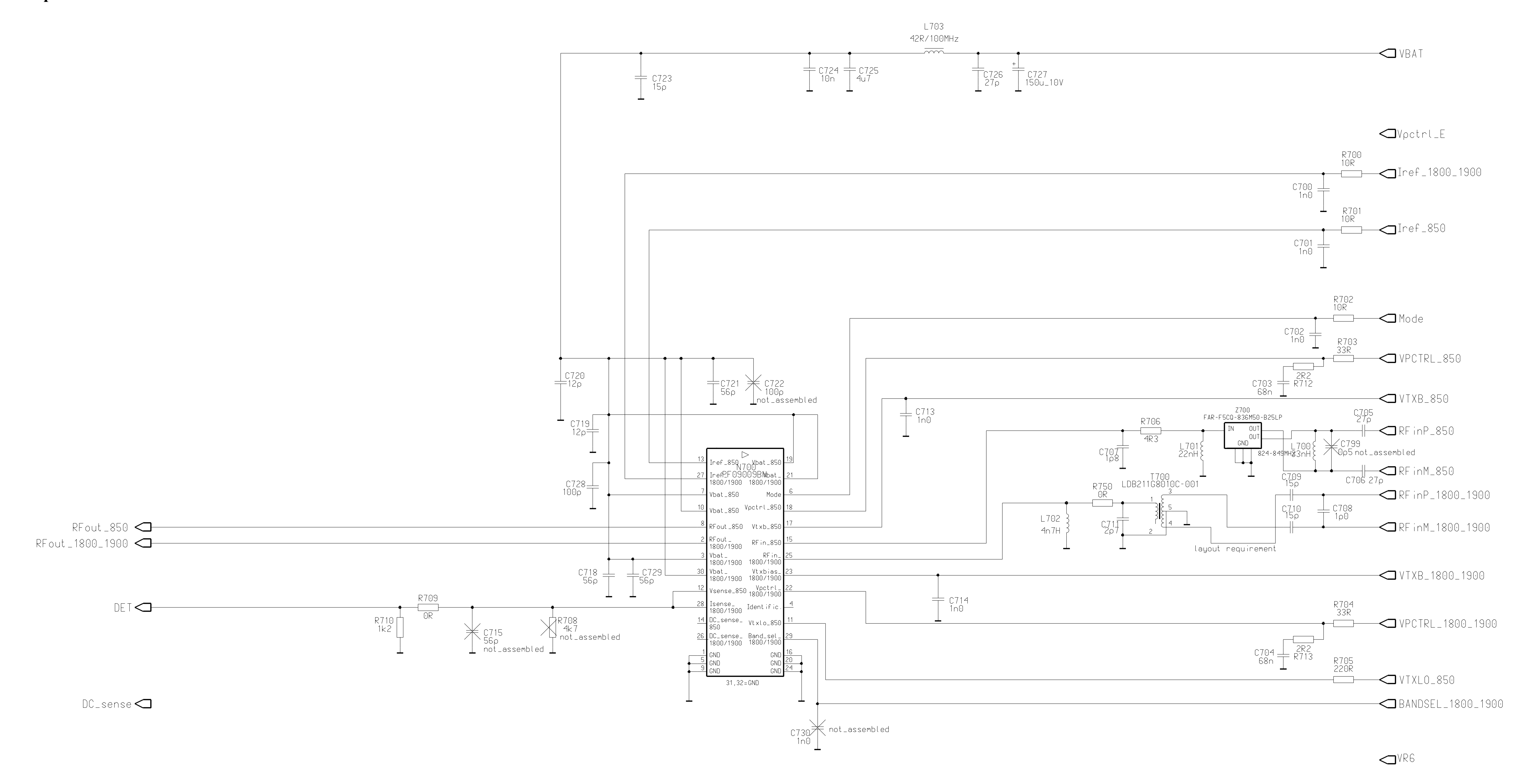
RF Block Diagram



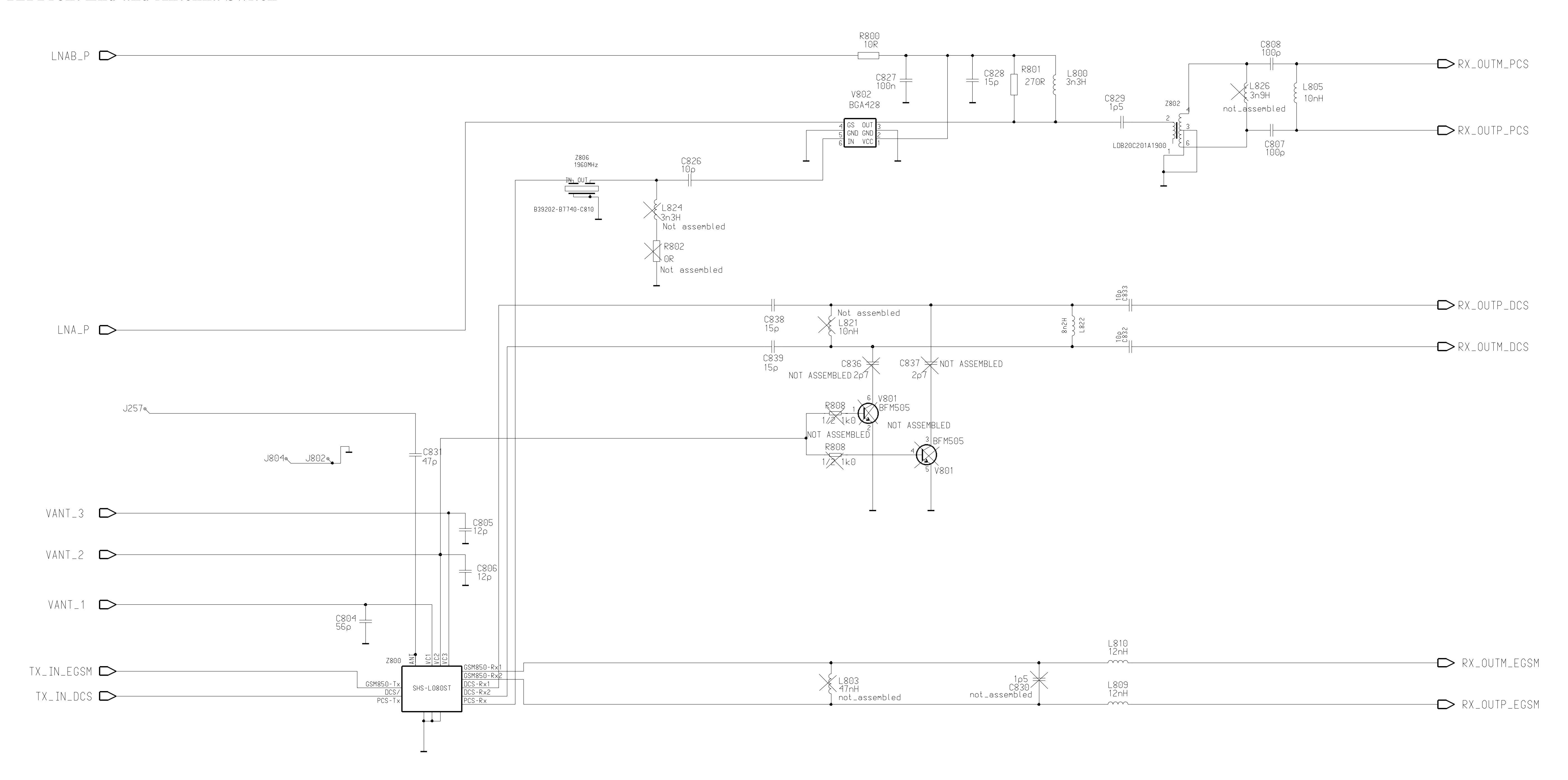
RF IC Helgo


N500
HELGO73A
T500
LDB213G6010C-001
G502
ENFVJ5W2S02
G501
XT20-KEU27L
26MHz
VR6
VR4
VR5
VR1
INP_G_RX
INM_G_RX
INP_D_RX
INM_D_RX
INP_P_RX
INM_P_RX
LNAB_G
LNAB_P
LNAB_D
LNA_P
VR7
VANT_3
VANT_1
VANT_2
VC_1
VC_2
VP_D_SEL
VB_DET
DET
VPCTRL_G
VPCTRL_P
Vpctrl_E
Iref_850
Iref_1800_1900
Mode
OUTP_G_TX
OUTM_G_TX
VR2
OUTP_P_TX
OUTM_P_TX
VTXLO_P
VTXLO_G
VTX_B_P
VTX_B_G
RXQ
RXI
VrefRF02
VrefRF01
RFBusData
RFBusClk
RFBusEna1
Reset
VR3
AFC
VCTCXOGnd
VCTCXO
TXC
TXP
TXA
TXIP
TXIM
TXQM
TXQP
RFTEMP
not_assembled

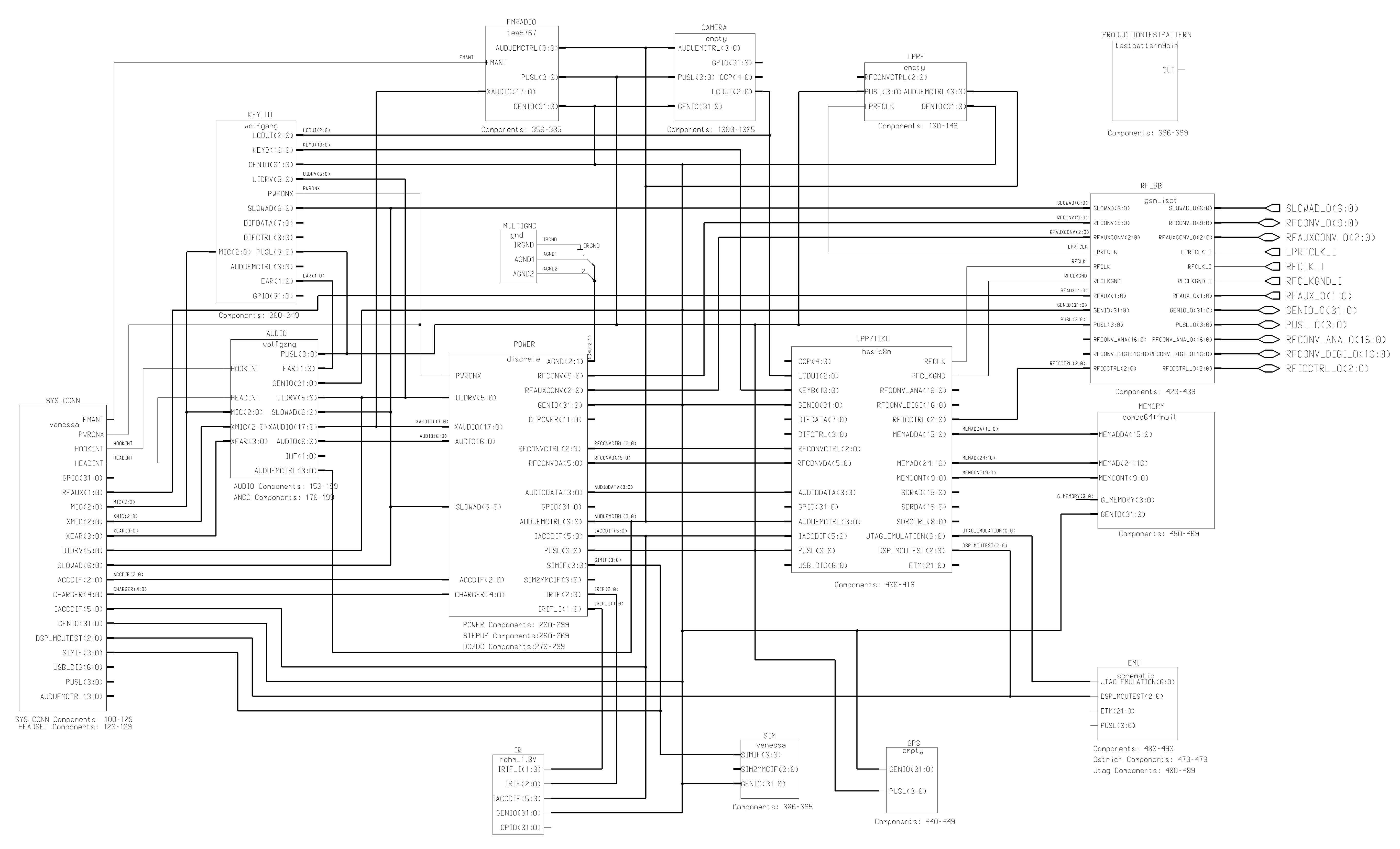
Power Amplifier Detection



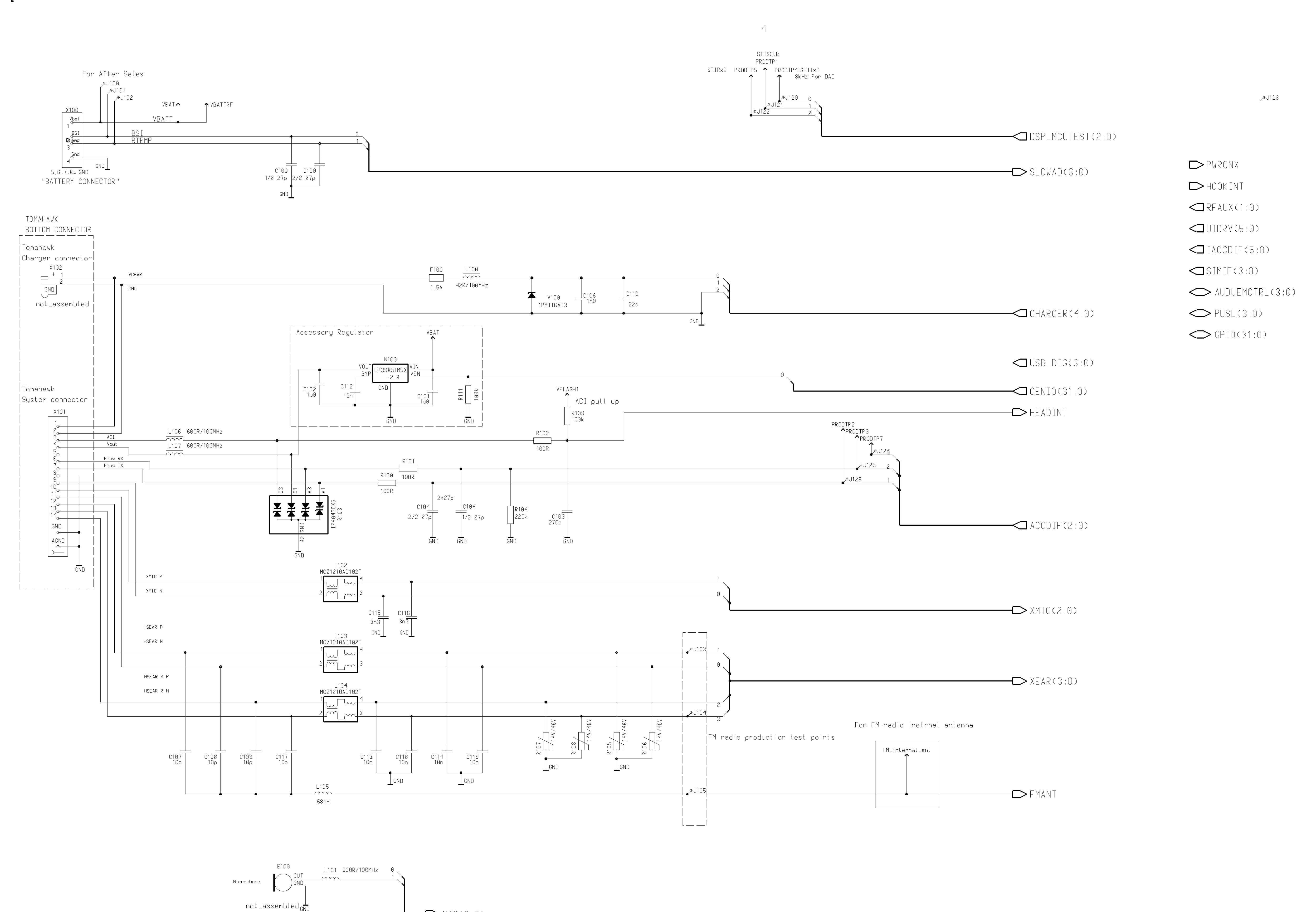
RX Front End and Antenna Switch



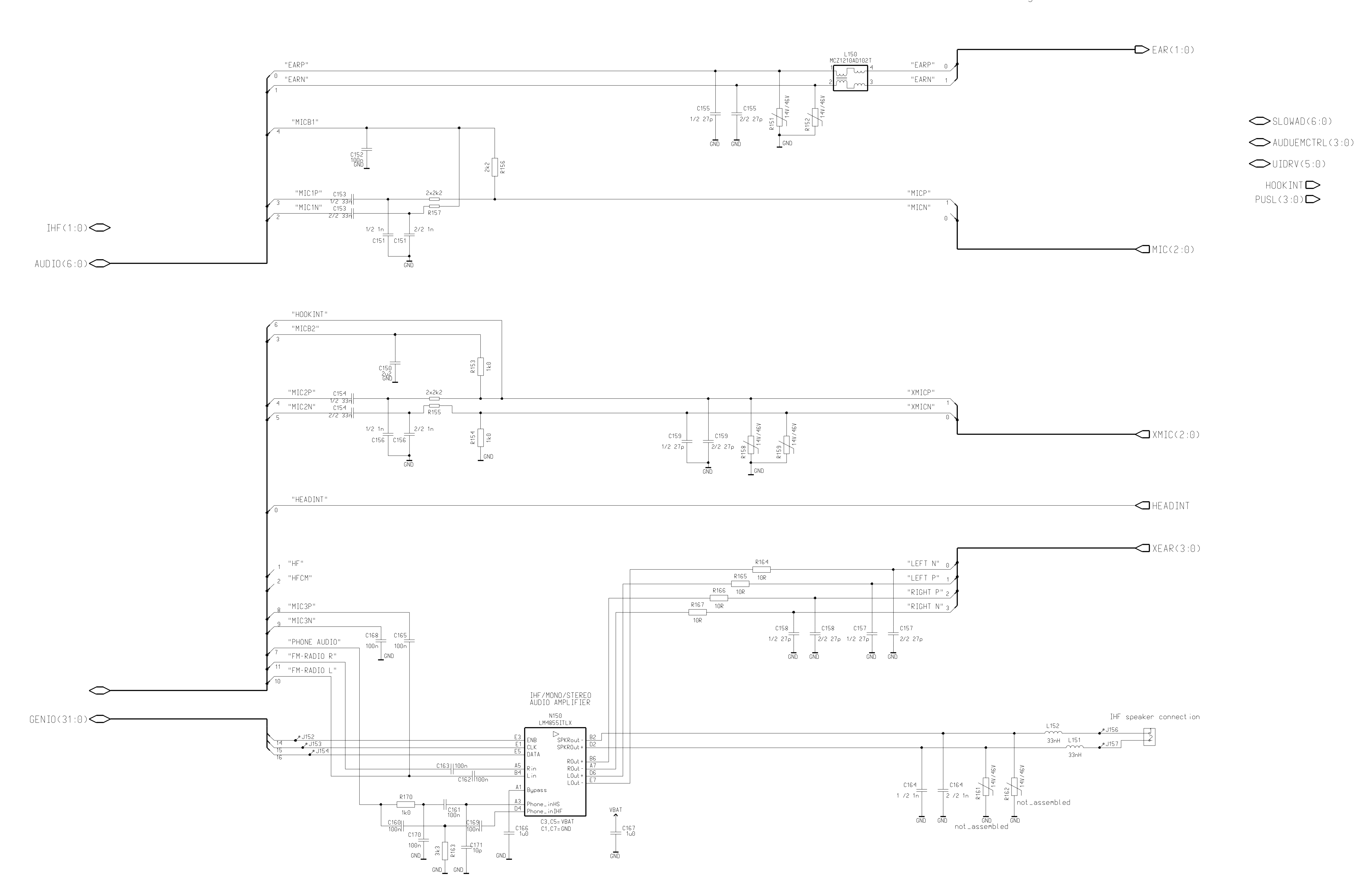
BB Block Diagram



System Connector

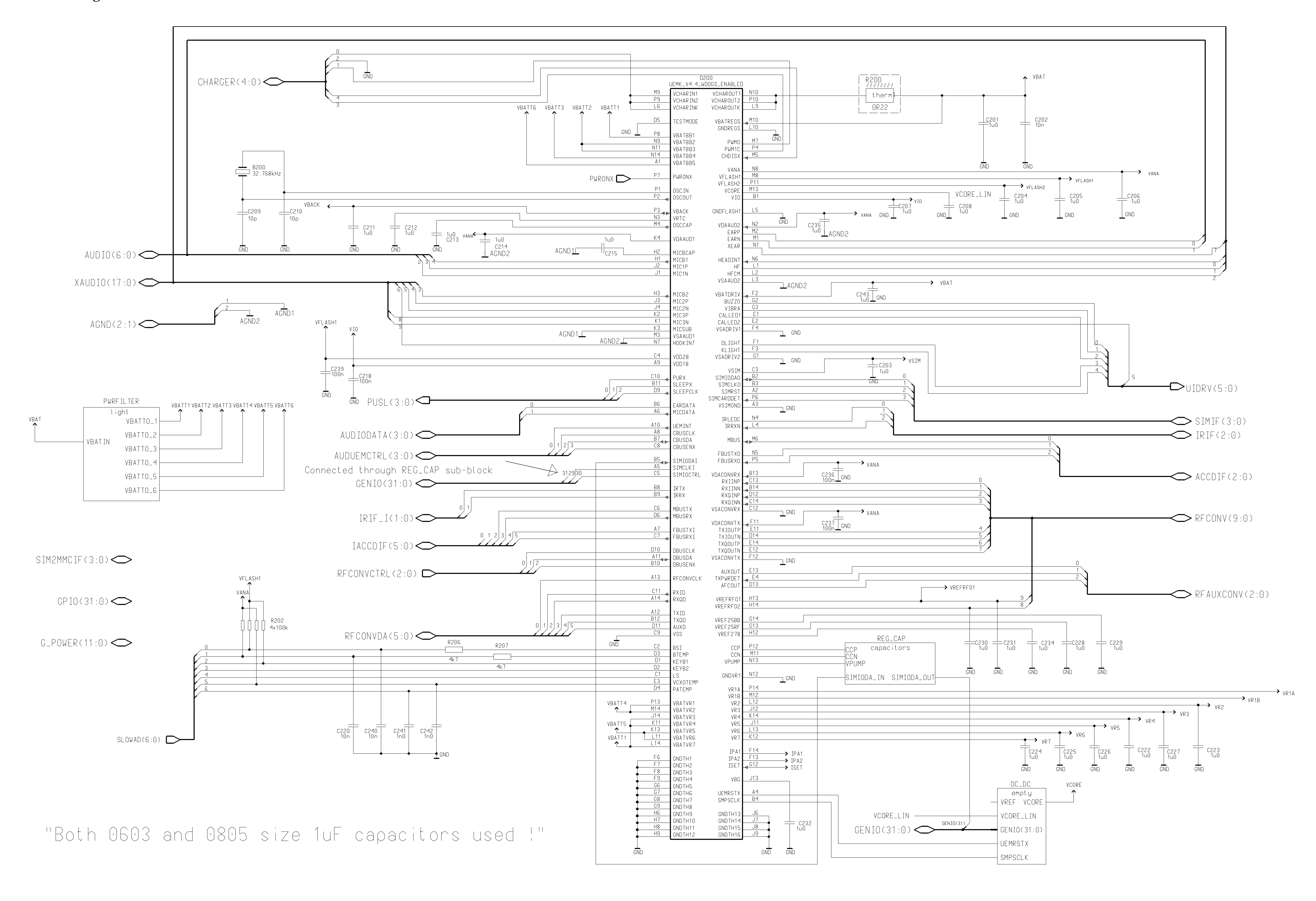


Audio

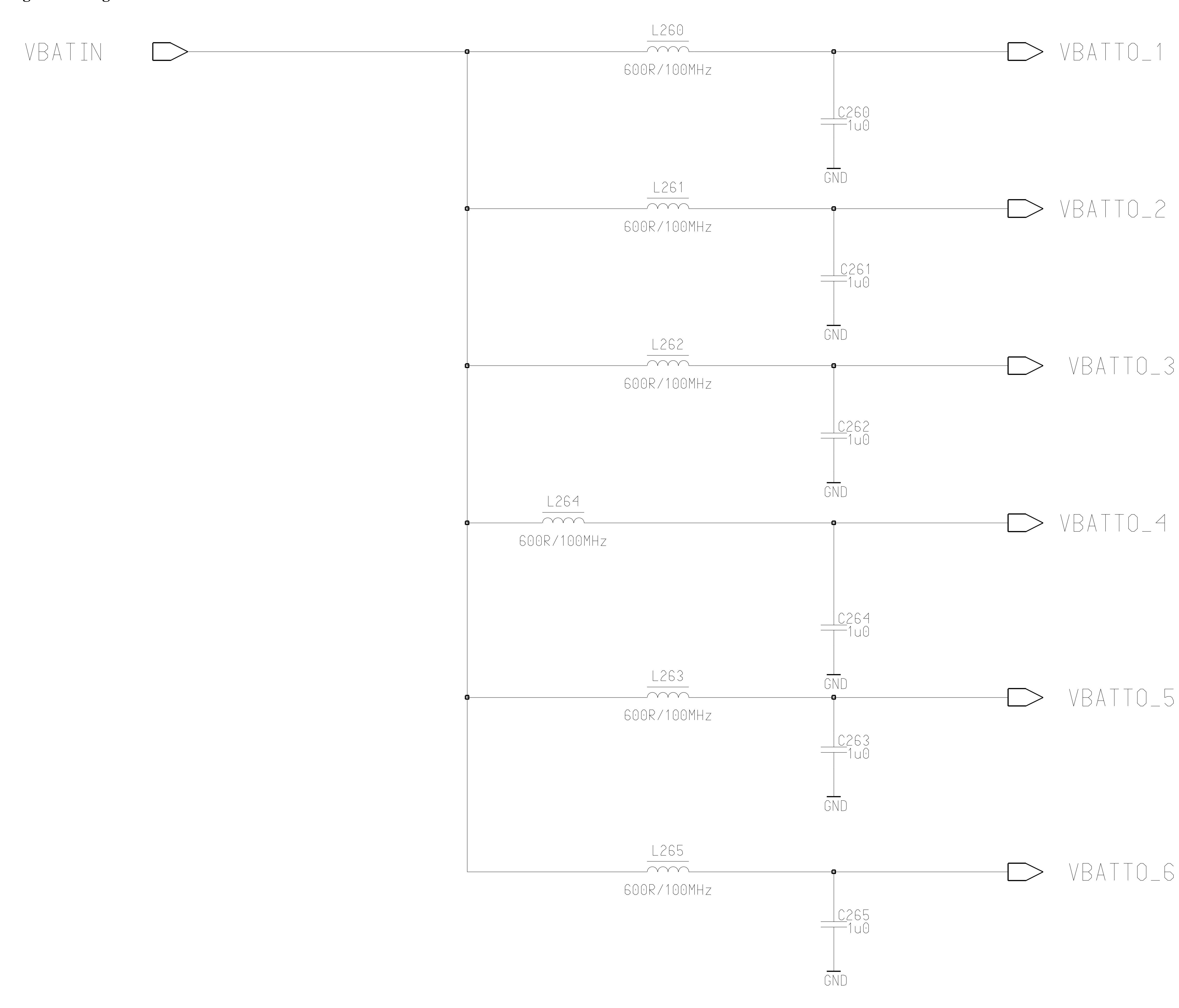

EAR(1:0)
MIC(2:0)
XMIC(2:0)
HEADINT
XEAR(3:0)
SLOWAD(6:0)
AUDUEMCTRL(3:0)
UIDRV(5:0)
HOOKINT
PUSL(3:0)
IHF(1:0)
AUDIO(6:0)
GENIO(31:0)
IHF/MONO/STEREO
AUDIO AMPLIFIER
N150
LM4855ITLX
IHF speaker connection
not_assembled

User Interface

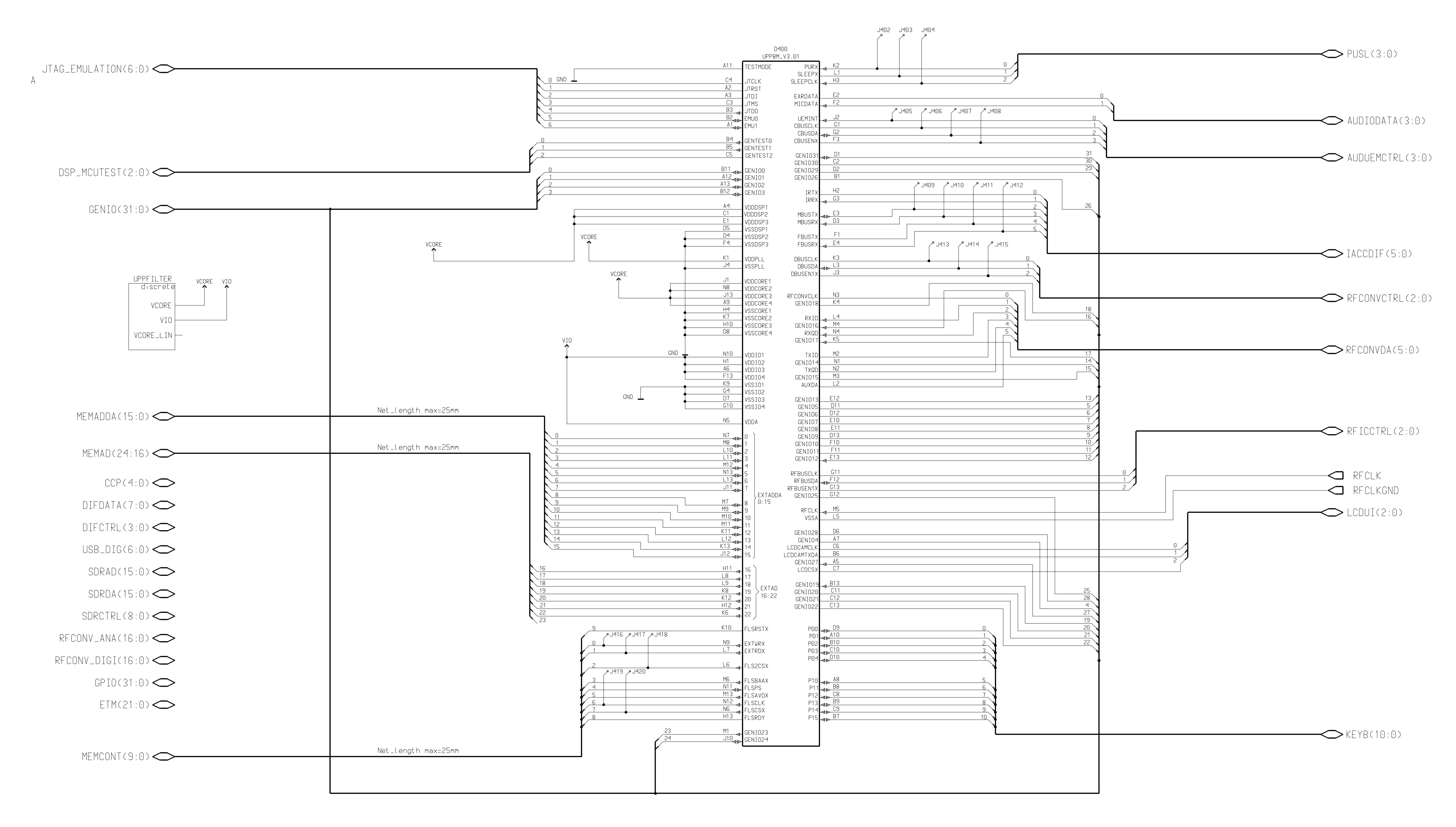
Power Management



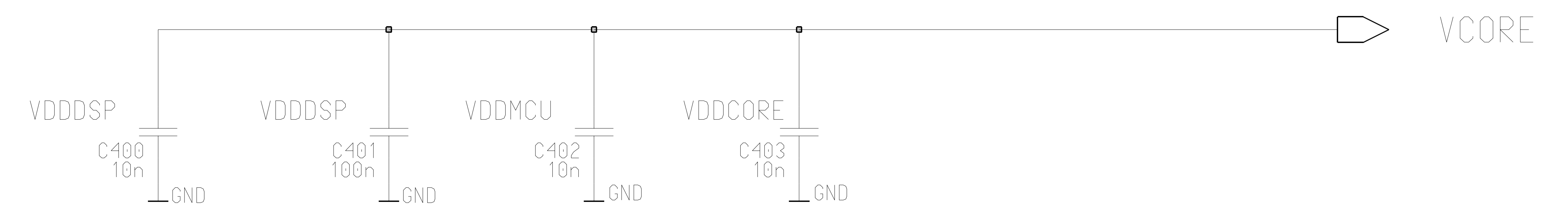
Light Filtering



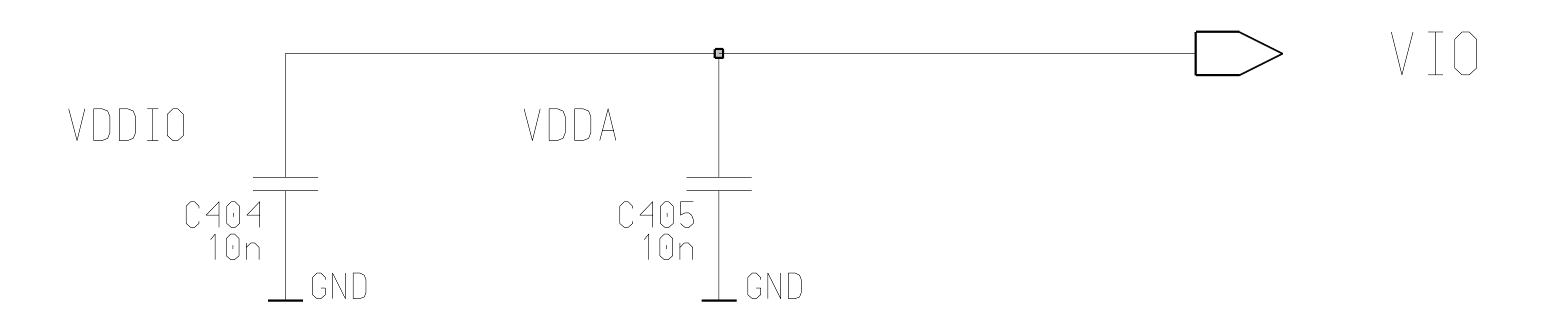
UPP 8M


JTAG_EMULATION(6:0)
DSP_MCUTEST(2:0)
GENIO(31:0)
MEMADDA(15:0)
MEMAD(24:16)
CCP(4:0)
DIFDATA(7:0)
DIFCTRL(3:0)
USB_DIG(6:0)
SDRAD(15:0)
SDRDA(15:0)
SDRCTRL(8:0)
RFCONV_ANA(16:0)
RFCONV_DIGI(16:0)
GPIO(31:0)
ETM(21:0)
MEMCONT(9:0)
PUSL(3:0)
AUDIODATA(3:0)
AUDUEMCTRL(3:0)
IACCDIF(5:0)
RFCONVCTRL(2:0)
RFCONVDA(5:0)
RFICCTRL(2:0)
RFCLK
RFCLKGND
LCDUI(2:0)
KEYB(10:0)
D400
UPP8M_V3.01
UPPFILTER
discrete
VCORE
VIO
VCORE_LIN
Net_length max=25mm

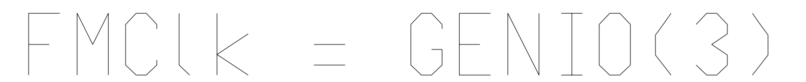
UPP Decoupling Capacitors



VCORE_LIN



FM Radio IC



GENIO(31:0)

N356
TEA5767HN

FMANT

FM_OUT
stereo_se
VAFR
VAFL
XAUDIO(17:0)

XAUDIO(17:0)

Components: 380-385

AUDUEMCTRL(3:0)

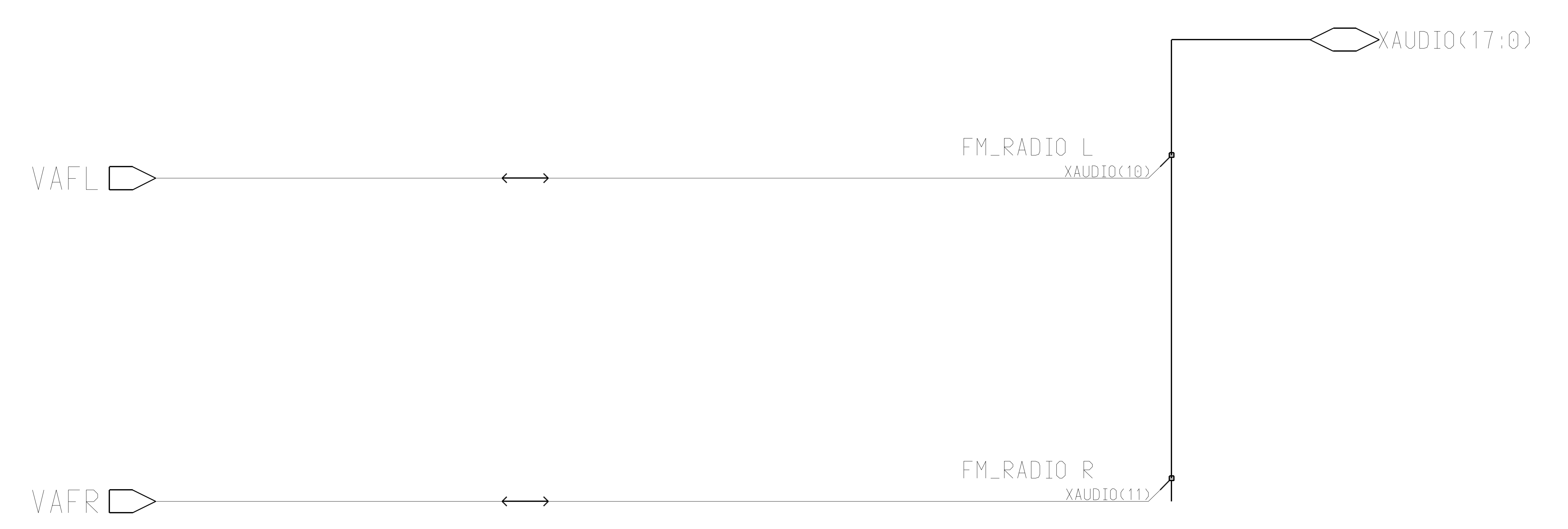
PUSL(3:0)

Notice:

C374 (1n0) and C375 (2n2) are configured for 32kHz reference clock

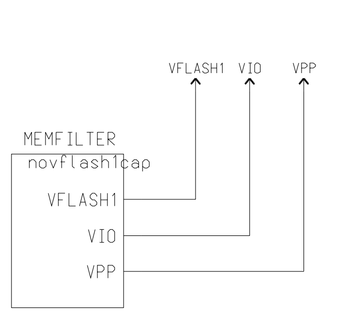
If reference clock is 6.5MHz, use C374 (3p9) and C375 (10p)

FM Radio Unit



Combo Memory

MEMEXTENSION
empty
MEMADDA(15:0)
MEMAD(24:16)
MEMCONT(9:0)
GENIO(31:0)
G_MEMORY(3:0)
FLS2CSX



MEMWING
empty
GENIO(31:0)
G_MEMORY(3:0)
MEMAD(24:16)
MEMADDA(15:0) FLS2CSX
MEMCONT(9:0) FLSCSX

GENIO(31:0) 23

D450
K5U6441BTM-TD90
FLASHM 4Mx16
SRAM 256kx16
MEMAD(16) B2 16
MEMAD(17) A9
MEMAD(18) B8 A
MEMAD(19) A8
MEMAD(20) B3 20
FLASH/SRAM
MEMAD(21) A2 A21/_LB
MEMAD(22) A10 A22/_UB
B7 _WP/_CS
FLASH
MEMCONT(6) A4 CLK RDY A1
MEMCONT(9) B6 _RESET
B9 _CEF
NC 1 E451
NC 2 E452
NC 3 E453
COMMON NC 4 E454
MEMCONT(5) B4 _AVD NC 5 E455
MEMCONT(0) A6 _WE NC 6 E456
MEMCONT(1) C10 _OE NC 7 E457
MEMCONT(4) B5 PS NC 8 E458

MEMAD(24:16)

D10 ADDRESS/DATA I/O
0 1 D9 2 C7 3 C6 4 D5 5 D4 6 C3 7 C2 8 C9 9 C8 10 D7 11 D6 12 C5 13 C4 14 D2 15 D1

VPP PRODTP6
MEMCONT(3) R450 4k7 E450

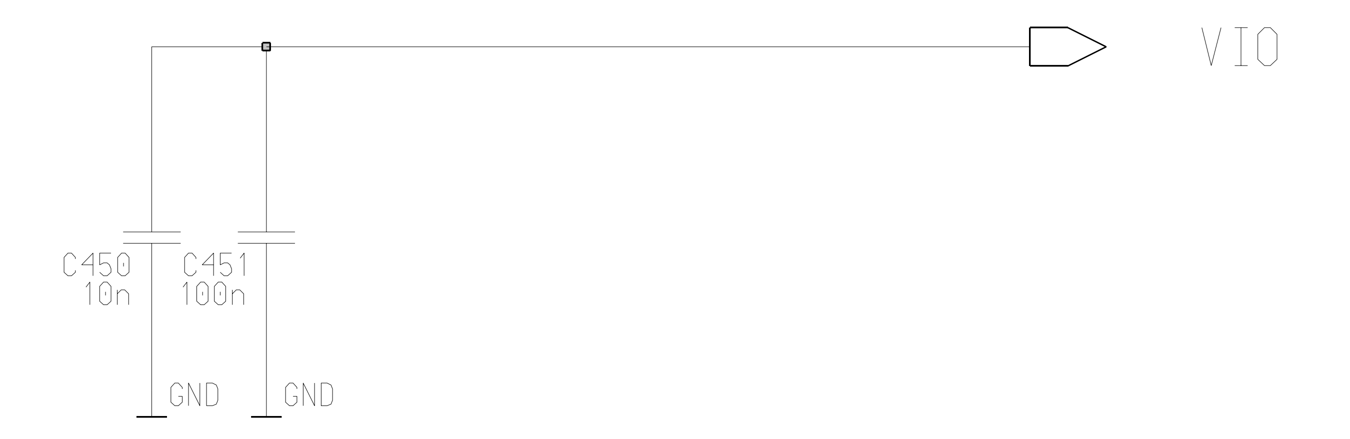
MEMCONT(9:0)
MEMCONT(8)

A5,B1,D8=VIO
A7= VPP
A3,B10,C1,D3=GND

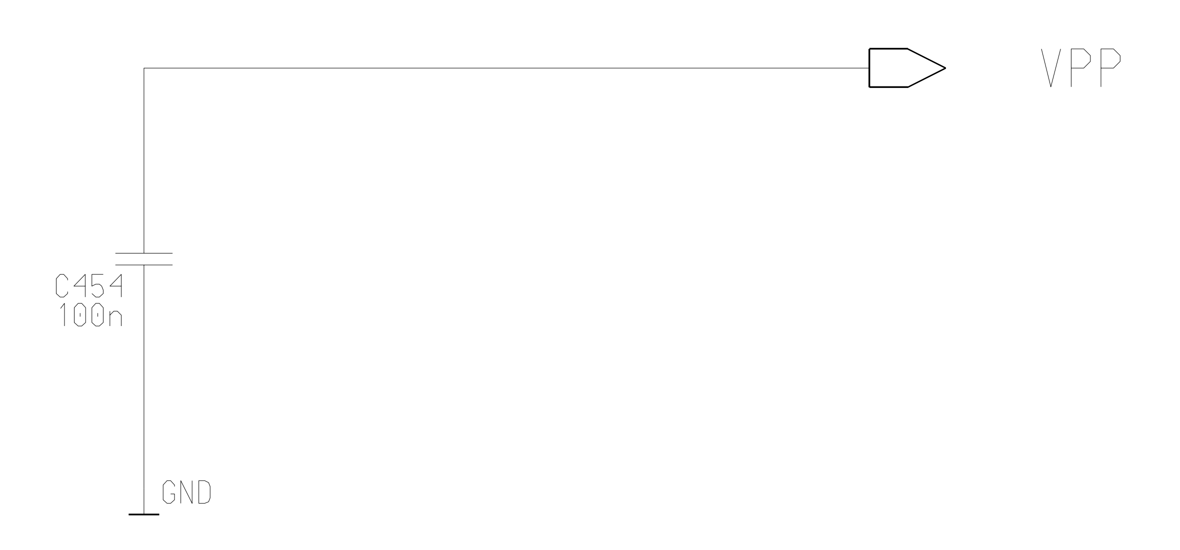
MEMADDA(15:0)

G_MEMORY(3:0)

Combo Decoupling Capacitors



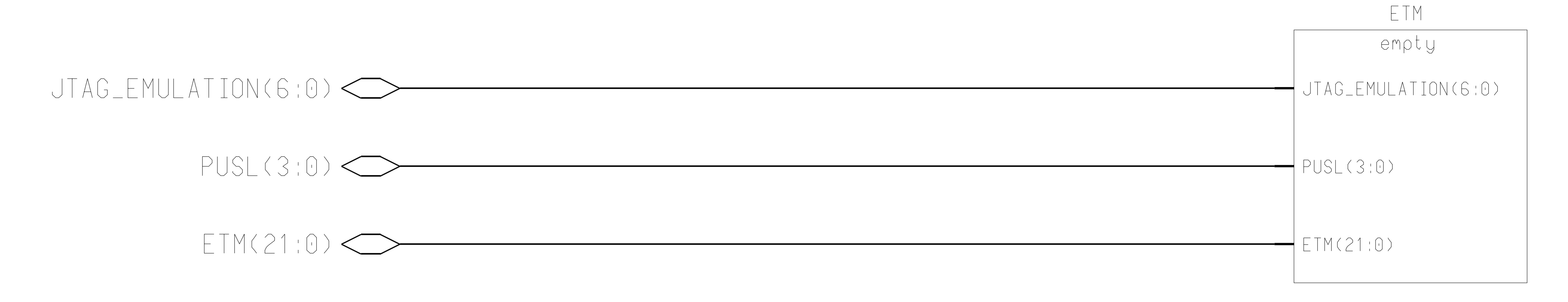
VFLASH1



Emulators

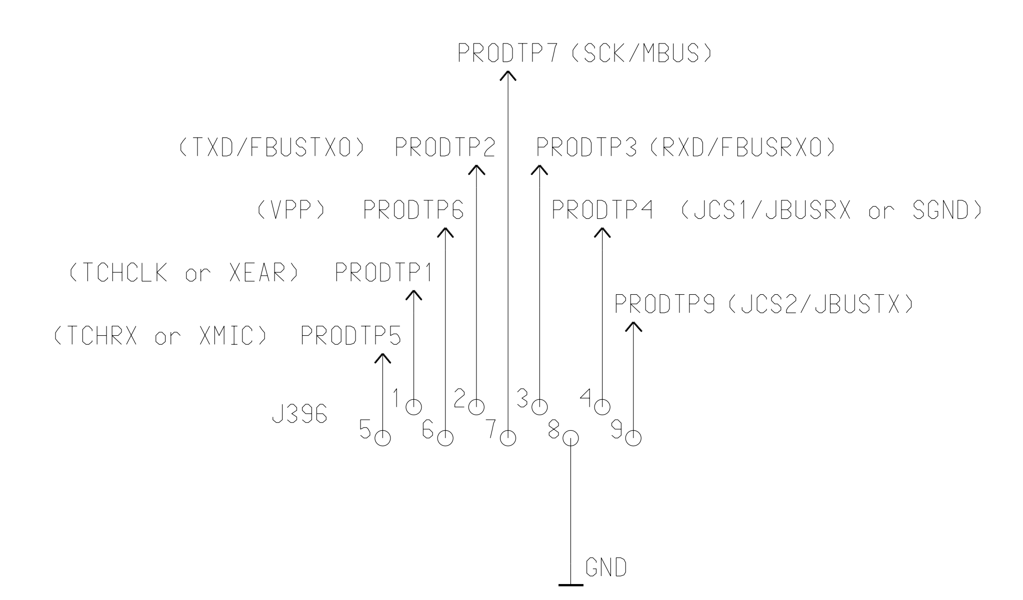

JTAG
empty
JTAG_EMULATION(6:0)
JTAG_EMULATION(6:0)


OSTRICH
connector
DSP_MCUTEST(2:0)
DSP_MCUTEST(2:0)

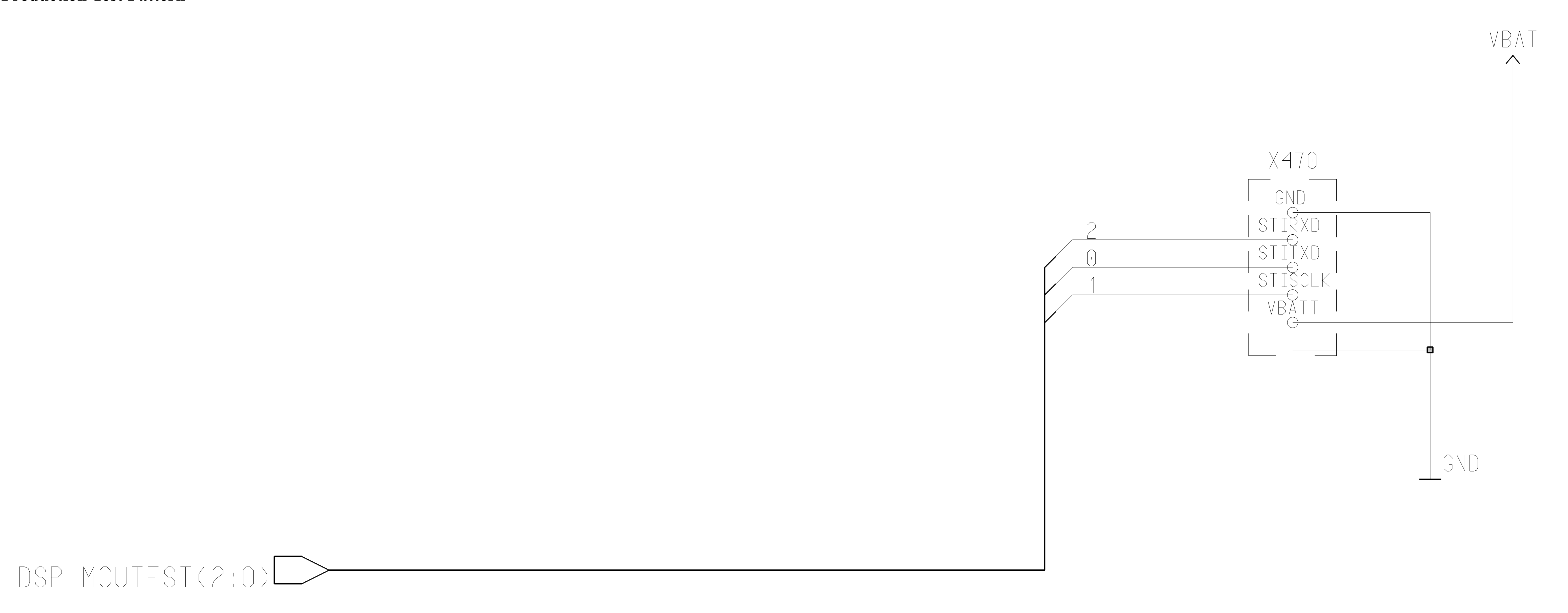

ETM
empty
JTAG_EMULATION(6:0)
PUSL(3:0)
ETM(21:0)
JTAG_EMULATION(6:0)
PUSL(3:0)
ETM(21:0)

Ostrich Emulator Connector

OUT

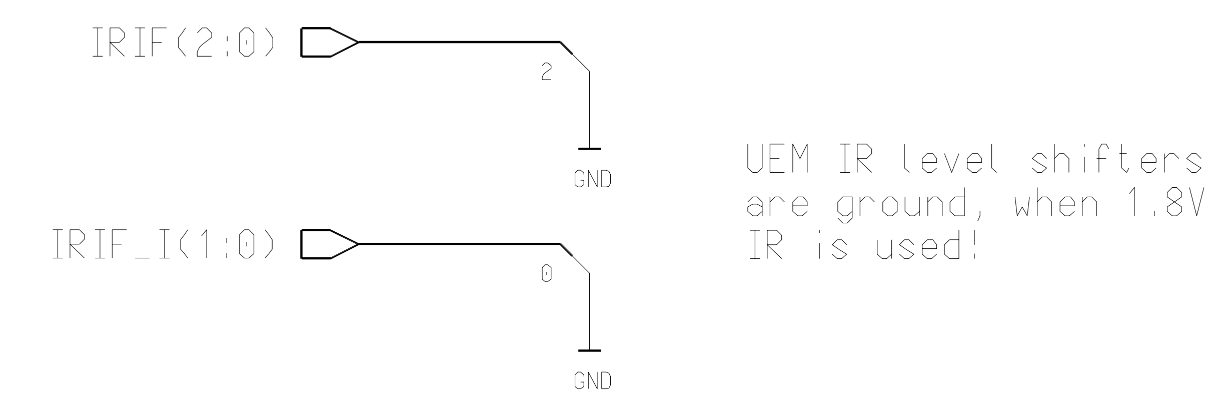


Production Test Pattern

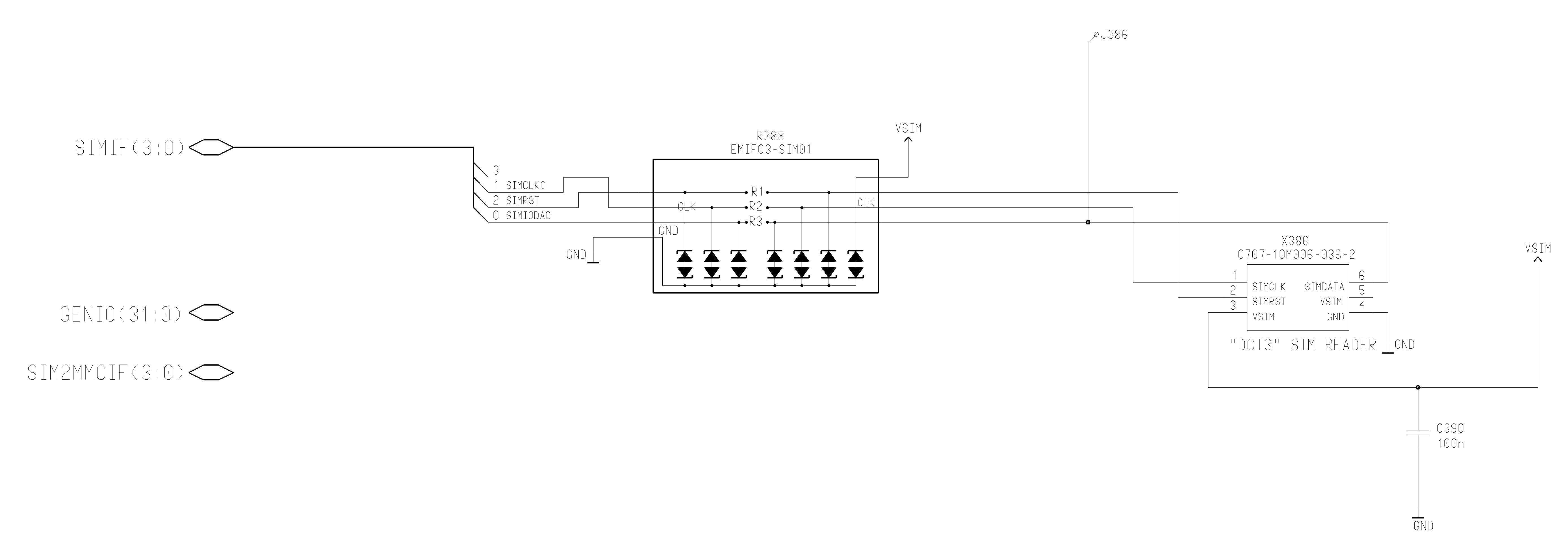


IR

IACCDIF(5:0)
GENIO(31:0)
GPIO(31:0)
1 RXD
10 SD
0 TXD
VFLASH1
VIO
VBAT
C350
4u7
IRGND
N350
RPM960-H7E3A
5 PWDWN
LEDA 1
IRED_A
3 TXD
RXD 4
6 Vcc
LEDC 2
GND 8
7 VIO
GND 9
R350
therm1
4R7
VFLASH1
C352
100n
C353
100n
C351
22p
For IR transceiver
IRGND
IRGND
IRGND
IRGND
not_assembled

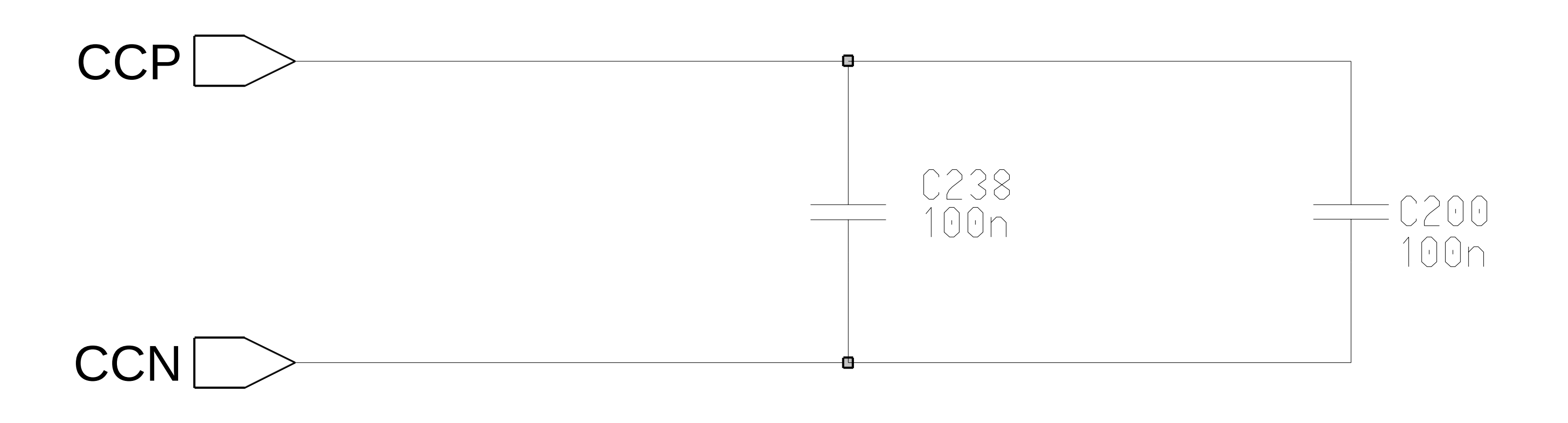


Sim Reader

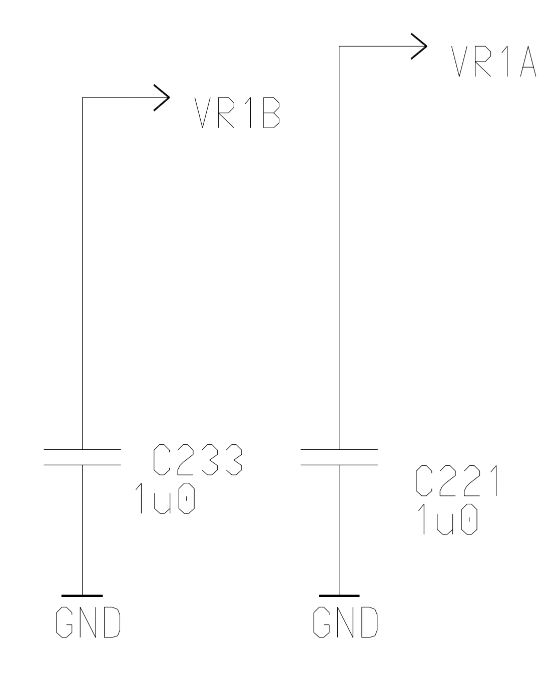

SIMIF(3:0)
GENIO(31:0)
SIM2MMCIF(3:0)
3
1 SIMCLKO
2 SIMRST
0 SIMIODAO
GND
R388
EMIF03-SIM01
CLK
R1
R2
R3
CLK
GND
VSIM
J386
X386
C707-10M006-036-2
1 SIMCLK
2 SIMRST
3 VSIM
SIMDATA 6
VSIM 5
GND 4
"DCT3" SIM READER
GND
VSIM
C390
100n
GND

Power Discrete

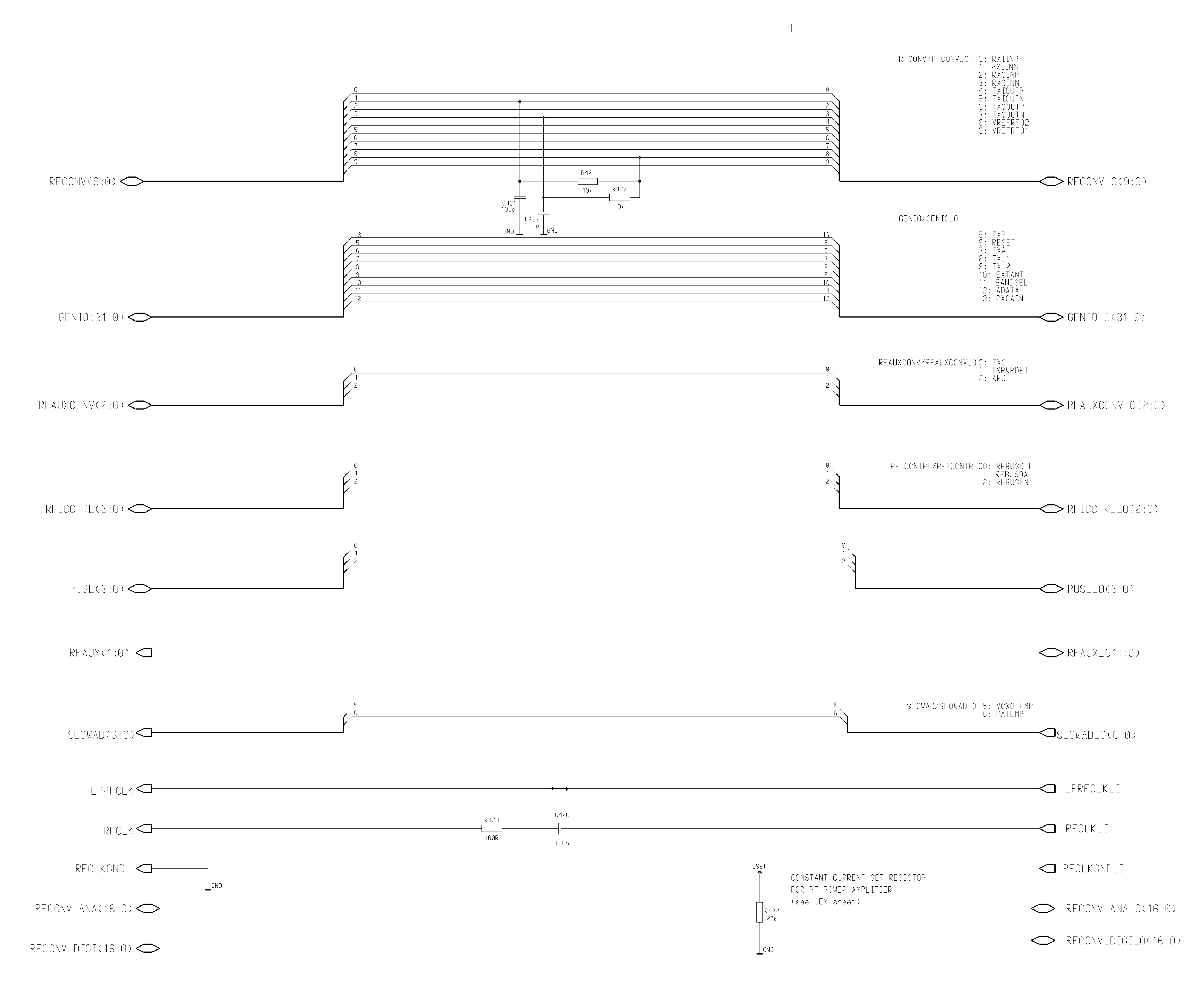








RF and BB Interface



IPA1 AND IPA2 ARE USED IN RF, THE TOLERANCE OF R422 IS 1% (0402, 1430873)